REMARKS

It was noticed when preparing this response that claims 14 and 15 were identical. Claim 14 has been cancelled above.

Claims 2-9, 11-13 and 15-21 are currently pending in this patent application.

Claims 2, 4, 5, 6, 8, 9, 11 and 13 are now rejected under 35 U.S.C. 102(e) as being anticipated by U.S. 6,249,560 (Ichihara, newly cited), and claims 3, 7, 12 and 14-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichihara. These rejections are respectfully disagreed with, and are traversed below.

Ichihara discloses in the prior art circuit of Fig. 4 a prescaler 5, and the same (unmodified) prescaler 5 is shown in Fig. 1. The goal of Ichihara is to reduce phase noise in the output of a PLL VCO that is generated by the frequency divider 7 (that is fed by the prescaler 5), as is made evident at, for example, col. 2, lines 18-21 and 40-42. There is no mention of reducing any noise generated by the prescaler 5 itself and, in fact, in the embodiment of FIGS. 2D, E and G, Ichihara state that the "prescaler 5 can be omitted" (col. 6, lines 47-49).

The applicants contend that the circuitry of Ichihara is incapable of reducing or removing noise in the prescaler 5 output signal since the triggering of the resampling circuit is performed after the prescaler 5 and, as a result, any noise and temporal ambiguity (jitter) in the output of the prescaler 5 signal will be present in the frequency divider 7 and at the flip-flop 9 triggering signal (clock signal C).

The applicants note further that VCO/PLL circuit noise can arise primarily from the asynchronously running frequency dividers and from the resulting temporal ambiguity or jitter in the edges of the prescaler output signal. The presence of the jitter in the output signal of the prescaler is manifested as circuit noise in downstream circuitry. A component of the noise can

also arise from spurious signals generated by the prescaler itself, such as when the prescaler modulus is changed when using a phase rotation or phase switching PLL topology.

It is further pointed out that the teachings of this invention enable a resampling prescaler to be constructed that overcomes the problems related to static, spurious signals generated by the prescaler. The conventional prescaler 5 of Ichihara would be incapable of overcoming such problems. For example, that the instant specification explains this situation at page 8, lines 19-22, as follows:

> "Note should be made that the teachings of this invention apply as well to the use of resampling to overcome problems introduced by systematical signals generated by a phase rotation modulus prescaler (e.g., systematic signals that are 1/4, 2/4 and 3/4 of the modulus cycle time (i.e., phase comparison frequency.))"

It is further noted that Ichihara makes no mention of a mobile phone application. If current consumption is not an issue, as it typically is a mobile phone application, the frequency divider after the prescaler may be dominant noise source.

Furthermore, Ichihara makes no mention of a modulus N prescaler, such as a dual modulus prescaler. This is significant, as spurious noise can be generated when the prescaler modulus is changed.

In view of the foregoing, it is clear that Ichihara is either not concerned with frequency jitter that can be generated by the prescaler 5 itself, or is unaware of its possible presence in the prescler 5 output signal.

Claim 2 is drawn to a phase locked loop that comprises a phase comparator that generates an output signal that is used to drive a voltage controlled oscillator, and further includes:

> "a modulus N prescaler circuit coupled to an output of said voltage controlled oscillator, said prescaler circuit comprising an input node for coupling to said

> output of said voltage controlled oscillator for receiving an input signal having a characteristic frequency to be divided by N, an output node for outputting a frequency divided signal that is coupled to said phase comparator, and a plurality of divider stages coupled between the input node and the output node for dividing the input signal by N, and further comprising at least one resampling stage coupled to an output of at least one of said divider stages for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal, thereby reducing temporal ambiguity in the occurrence of the edges of the output signal" (emphasis added).

The circuit elements 5, 7, 9 and 11 of Ichihara are clearly not a "modulus prescaler" as stated by the Examiner (only the block 5 is the (conventional) prescaler), and thus the Examiner's analysis of the disclosed circuitry is fundamentally flawed. This being the case, at least the highlighted text appearing in claim 2 is not disclosed or suggested by Ichihara, and thus Ichihara clearly cannot anticipate claim 2, nor does Ichihara make the subject matter of claim 2 obvious or otherwise unpatentable.

In that claim 2 is clearly allowable over the disclosure of Ichihara, then dependent claim 4 is allowable as well.

Independent claim 5 is drawn to a method for reducing power consumption in a frequency source of a mobile station, and comprises:

> "operating a phase locked loop as part of the frequency source to generate a signal having a desired frequency, the step of operating the phase locked loop including a step of dividing a frequency of an output signal of a voltage controlled oscillator by a predetermined amount to generate a frequency divided signal; and
>
> resampling the frequency divided signal using a flip-flop circuit that has a data input coupled to said frequency divided signal and a clock input that is clocked with the output signal of the voltage controlled oscillator to reduce jitter in the frequency divided signal" (emphasis added).

As was argued above, Ichihara does not mention a mobile station, nor is there any mention of

power consumption reduction. Furthermore, an inspection of FIG. 1 shows that the flip-flop circuit (either 9 or 10) is not clocked with the output of the VCO 4.

Claim 5 is clearly not anticipated by, nor made obvious in view of, the disclosure of Ichihara.

Dependent claim 6 is also clearly allowable in that it depends from allowable claim 5. Furthermore, and as was argued above, there is no disclosure by Ichihara of a step of resampling that operates:

> "a modulus N prescaler circuit that is coupled to the output of the voltage controlled oscillator, the prescaler circuit comprising an input node for coupling to the output of the voltage controlled oscillator for receiving an input signal having a characteristic frequency to be divided by N, an output node for outputting a frequency divided signal that is coupled to a phase comparator of the phase locked loop, and a plurality of the frequency divider circuits coupled between the input node and the output node for dividing the input signal by N, where the step of resampling is accomplished in a resampling stage coupled to an output of at least one of the frequency divider circuits for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal, thereby reducing jitter of the output signal" (emphasis added).

Dependent claim 8 is thus also clearly allowable.

Independent claim 9 is drawn to a method to operate a phase locked loop as part of a frequency source to generate a signal having a desired frequency, and comprises:

> "operating a multi-modulus prescaler function of the phase locked loop to divide a frequency of an output signal of an oscillator by a predetermined amount to generate a frequency-divided signal; and
>
> resampling the frequency divided signal using a flip-flop circuit that has a data input coupled to the frequency divided signal and a clock input that is clocked with the output signal of the oscillator" (emphasis added).

Based on the argument presented above, the circuit elements 5, 7, 9 and 11 of Ichihara are clearly not a "multi-modulus prescaler" as stated by the Examiner (only the block 5 is the (conventional) prescaler), and thus again the Examiner's analysis of the disclosed circuitry is fundamentally flawed. Furthermore, and as was also argued above, in FIG. 1 the flip-flop circuit 9 is not clocked with the output of an oscillator, but is clocked instead with the (inverted) output of the prescaler 5. This being the case, at least the highlighted text appearing in claim 9 is not disclosed or suggested by Ichihara, and thus Ichihara clearly cannot anticipate claim 9, nor does Ichihara make the subject matter of claim 9 obvious or otherwise unpatentable. Dependent claims 11 and 13 are thus also clearly allowable over Ichihara, at least for the reasons argued above with respect to claims 6 and 8.

Claims 3, 7 and 12 are clearly not rendered unpatentable over Ichihara, as there is no mention of a modulus N or multi-modulus prescaler 5 in Ichihara, and thus clearly no mention of a programable modulus N or multi-modulus prescaler. Furthermore, and even if the prescaler 5 of Ichihara were a programmable modulus N or multi-modulus prescaler, which is not admitted is suggested by Ichihara, there would still be no suggestion that the output signal of the prescaler 5 would in any way have reduced temporal ambiguity in the occurrence of the edges of the output signal (e.g., as in claim 1), or that jitter in the output signal of the prescaler 5 would in any manner be reduced (e.g., as in claim 5).

Dependent claims 15 and 16 are clearly allowable over Ichihara, at least for the reason that each depends from allowable claim 9.

Independent claim 17 is drawn to a mobile station that comprises a RF transceiver that is tunable using a frequency synthesizer that comprises a PLL, where the PLL comprises a phase comparator for comparing a frequency divided oscillator output signal to a frequency divided VCO output signal. The PLL further comprises:

> "a prescaler block disposed between an output of said VCO and an input of a frequency divider, said prescaler block comprising a frequency divider block

having an input coupled to said output of said VCO, said frequency divider block having an output for outputting a frequency divided signal, said prescaler block further comprising a flip-flop having an input coupled to said output of said frequency divider block and a clock input coupled to said output of said VCO, said flip-flop operating to cause said prescaler block to output to said frequency divider a prescaled VCO signal having edge transitions that are synchronized to edge transitions of the VCO output signal."

In accordance with the foregoing arguments it should be clear at this point that Ichihara does not expressly disclose or suggest that their prescaler 5 forms a part of PLL of a mobile station frequency synthesizer, nor does Ichihara disclose that the prescaler 5 comprises circuitry that would suggest at least the underlined text above. This being the case, claim 17 is clearly allowable over the disclosure of Ichihara, as are claims 18-21 that depend from claim 17.

The Examiner is respectfully requested to reconsider and remove the final rejections based on Ichihara, and to allow all of the now pending claims 2-9, 11-13 and 15-21.

Respectfully submitted:

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